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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/634,758 | 08/06/2003 | Yuji Nakagawa | 108075-00114 | 6859 |

4372 7590 11/01/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| NGUYEN, THAN VINH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2187 | |

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/634,758 | NAKAGAWA, YUJI | |
| | Examiner | Art Unit | |
| | Than Nguyen | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *3/30/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/04, 3/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-30 are pending.

2. The IDSes, filed 1/30/04 and 3/30/04, have been considered.

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Memory Device And Method For Arbitrating Internal And External Access.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizugaki et al (US 6,545,943).

As to claims 1,18,19,21,25,29

7. Mizugaki teaches the claimed semiconductor memory device and its method of operation comprising: an arbiter which receives a first entry signal for entering the first access mode and a second entry signal for entering the second access mode, and determines priority of the first and

second access modes in accordance with an order of receipt of the first and second entry signals, and sequentially generates a first mode (read/write access) trigger signal corresponding to the first entry signal and a second mode (internal refresh) trigger signal corresponding to the second entry signal in accordance with the determined priority (block controller 7/44-53); and a signal generating circuit, connected to the arbiter, for generating an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal, wherein the arbiter executes the first access mode by priority over the second access mode, when the arbiter is supplied with the first entry signal within a predetermined period after priority for the second access mode has been determined (determine priority of request; Abstract; 3/34-52, 5/34-67, 6/34-44).

As to claim 2:

8. Mizugaki teaches the arbiter determines whether the first entry signal has been supplied within the predetermined period or not in accordance with the internal operation signal (2/33-38; 3/45-53).

As to claim 3,13,14,20:

9. Mizugaki teaches the semiconductor memory device includes a plurality of word lines, and the internal operation signal is used as a decision signal indicating whether or not a predetermined word line is enabled in the second access mode (if internal refresh, external request is disabled; 5/33-63).

As to claim 4:

10. Mizugaki teaches the semiconductor memory device includes a plurality of word lines, and the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode (refresh mode determine if word line is enabled/disabled; Abstract; 5/63-67).

As to claim 7:

11. Mizugaki teaches the arbiter includes: a first decision circuit which receives the first entry signal and the second entry signal and determines priority of the first and second access modes in accordance with the order of receipt of the first and second entry signals (7/44-56), a second decision circuit, connected to the first decision circuit, for determining whether the first entry signal has been supplied within the predetermined period or not (2/33-38), and a mode trigger generating circuit, connected to the first decision circuit, for generating the first mode trigger signal in accordance with the determined priority (5/33-67), and wherein the mode trigger generating circuit generates the first mode trigger signal when the first entry signal is supplied to the second decision circuit within the predetermined period (2/33-38).

As to claim 8:

12. Mizugaki teaches the second decision circuit generates a cancel signal for stopping execution of the second access mode when the first entry signal is supplied within the predetermined period (2/33-38).

As to claim 9,23:

13. Mizugaki teaches after generating the cancel signal, the second decision circuit generates the second entry signal again to execute the second access mode after execution of the first access mode (activate word line for external write; 2/35-38).

As to claim 5,6,10,24:

14. Mizugaki teaches an address generating circuit for generating an address to be used for the second access mode, and wherein the address generating circuit does not generate the address when the arbiter determines the first access mode has priority (during refresh, external address is not enabled; 5/53-67).

As to claim 11:

15. Mizugaki teaches the arbiter includes a time setting unit which determines whether the first entry signal has been supplied within the predetermined period or not (abstract; 2/33-38).

As to claim 12,15,30:

16. Mizugaki teaches the device has a test mode and further comprises an exclusive test terminal to which the second entry signal for the test mode is supplied (Fig. 4 has input for external request).

As to claim 16:

17. Mizugaki teaches the first access mode is a read or write operation mode and the second access mode is a self-refresh operation mode (read/write or refresh access; 5/46-67).

As to claim 17,26,27,28:

18. Mizugaki teaches the semiconductor memory device includes a plurality of word lines, the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode (external access; 5/33-68), and the predetermined period comprises a period from a point at which the second entry signal is enabled prior to enabling of the first entry signal to a point at which the word-line enable signal is enabled (abstract; 2/33-38, 6/33-44).

As to claim 22:

19. Mizugaki teaches executing the first access mode includes stopping execution of the second access mode (external access after refresh 5/53-6/15).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Than Nguyen can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen
Primary Examiner
Art Unit 2187